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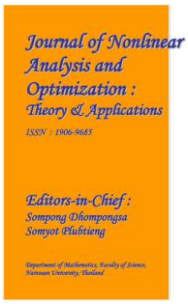

AN OVERVIEW OF THE DESIGN OF CMOS OPERATIONAL AMPLIFIERS AND THEIR USES IN BIOLOGY

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ABSTRACT
The relevance of using biomedical technology and wearable electronics for continuous illness diagnosis, monitoring, and therapy has increased significantly in recent years. This trend is driven by the need for more personalized and continuous healthcare solutions, especially for chronic diseases. Electrical and microelectromechanical technologies play a crucial role in the quickly evolving healthcare industry by enabling the development of innovative devices and systems.
Intelligent devices and well-designed circuits can lead to improved healthcare facilities and shorter hospital stays. For example, wearable devices can continuously monitor vital signs and other health parameters, providing real-time data to healthcare providers and patients. Additionally, some devices can be implanted within the body, allowing for continuous monitoring and treatment without the need for frequent hospital visits.
One of the key challenges in developing these devices is creating communication links, especially for implanted devices. Wireless technologies are essential for enabling communication between these devices and external systems. Power amplifiers are critical components of the transmitters in these devices, and their efficient operation is vital for ensuring reliable communication.
In recent years, there has been a significant increase in the development of implanted electronic devices for disease monitoring and diagnostics. These devices are designed to provide continuous monitoring of various physiological parameters and can transmit data wirelessly to external devices for further analysis. This continuous monitoring can help healthcare providers detect and diagnose diseases at an early stage, leading to better treatment outcomes.
Keywords: amplifiers; biomedical applications; disease; implantable amplifier designs; industrial;scientific; medical (ISM) bands; patient

INTRODUCTION

Operational amplifiers (op-amps) are essential components in analog electronic circuits, providing critical functions such as amplification, filtering, and signal conditioning. In the context of CMOS technology, op-amps are particularly important due to their widespread use in integrated circuits for various applications, including telecommunications, medical devices, computers, and consumer electronics.

Trends in Low-Voltage, Low-Power Silicon Chip Systems: The trend towards low-voltage, low-power silicon chip systems has been driven by the increasing demand for smaller size and longer battery life in portable applications. This trend has led to the development of more efficient and compact op-amp designs to meet the requirements of modern electronics. These designs aim to achieve high performance while minimizing power consumption and chip area.

Importance of Op-Amps in Analog Electronic Circuits: Op-amps are versatile devices that can be configured in various ways to perform a wide range of analog signal processing tasks. They are used in circuits ranging from simple bias generation to complex high-speed amplification and filtering. Op-amps are among the most widely used electronic devices today, being used in a vast array of consumer, industrial, and scientific devices.

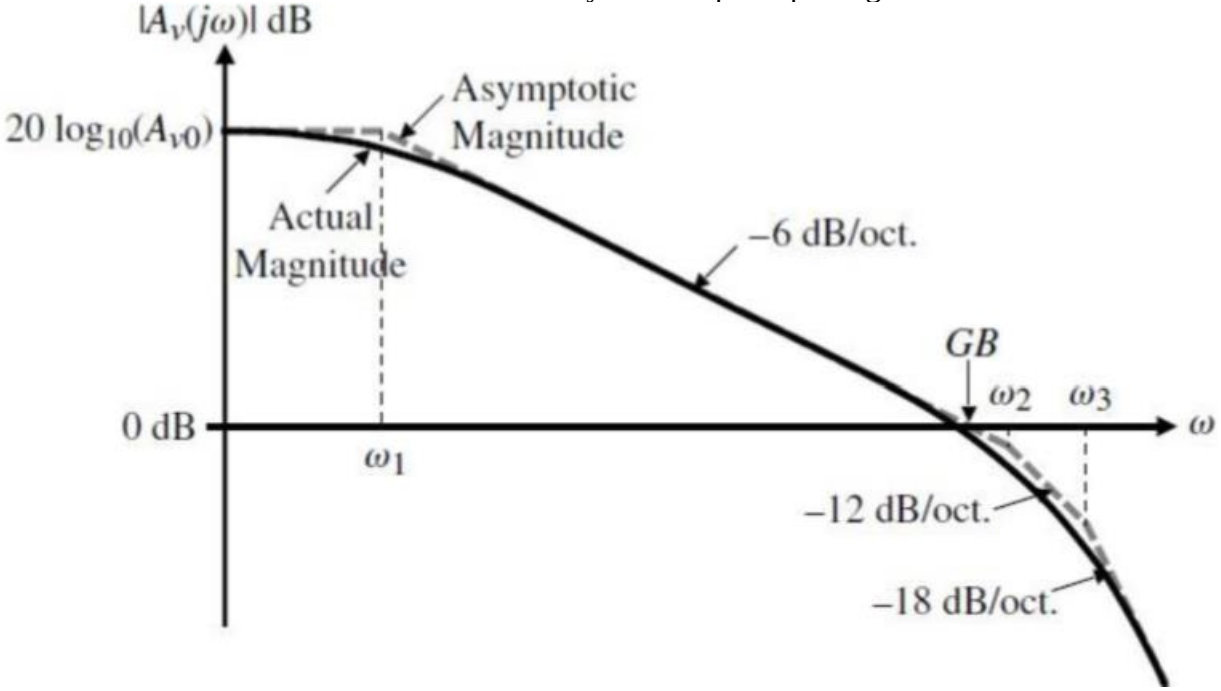
Design Case Study: In a specific design case study, a two-stage op-amp was developed with internal compensation using negative Miller capacitance in the first stage and Miller capacitance in the second stage. This approach was chosen to ensure circuit stability using Miller compensation while increasing bandwidth using negative Miller compensation. The op-amp was designed using the gm/ID ratio design approach, which is a common method for designing low-voltage, low-power op-amps. This approach involves optimizing the transconductance-to-drain current ratio (gm/ID) of the MOSFETs in the amplifier to achieve the desired performance metrics, such as DC gain, unity gain frequency, phase margin, and gain margin.

Simulation and Performance Evaluation: Simulation using Cadence Spectre simulator was used to assess the AC performance of the op-amp both with and without an output load capacitance. This simulation helps to ensure that the op-amp meets the design requirements for bandwidth, gain, and stability under different operating conditions. The design and implementation of CMOS operational amplifiers are critical for meeting the demands of modern portable applications, and the development of efficient and compact op-amp designs is essential for achieving smaller size, longer battery life, and improved performance in these applications.

Operational amplifiers (Op-Amps) play a crucial role as a significant circuit building block in electronic circuit designs. These components serve as input differential amplifier circuits that utilize external feedback to construct various practical circuits, including comparators, buffers, oscillators, filters, and instrumentation amplifiers, among others. Over recent years, there has been a notable trend towards operating Op-Amps at lower power supply voltages, particularly for portable applications, while also employing single rail operation and utilizing lower geometry fabrication processes.

However, reducing the supply voltage and transistor sizes can have significant implications for the design characteristics of operational amplifiers, particularly in terms of stability and frequency response. Lowering the supply voltage affects the operating range and headroom of the Op-Amp, potentially impacting its performance and dynamic range. Additionally, operating at lower voltages may introduce challenges related to noise margins and signal-to-noise ratio, requiring careful consideration during the design process.

Furthermore, utilizing lower geometry fabrication processes can lead to increased transistor densities and improved performance in terms of speed and power consumption. However, it also introduces challenges related to device mismatch, process variations, and reliability issues, which must be addressed to ensure the robustness and reliability of the Op-Amp design.



Typical Frequency Response of an Op-Amp

In the pursuit of designing operational amplifiers (Op-Amps) suitable for portable applications, various design concepts and circuit architectures have been considered to address performance-

related issues. One common technique employed is Miller compensation, which is used to improve the stability and frequency response of the Op-Amp.
The general block diagram of a two-stage Op-Amp, which incorporates Miller compensation, is illustrated in Figure 1. This diagram typically consists of several key components, including input differential pairs, gain stages, and output stages, along with compensation components to enhance stability and performance. Miller compensation is often applied in the first and/or second stages of the Op-Amp to optimize its response characteristics.
By carefully designing the architecture and incorporating appropriate compensation techniques, designers can mitigate performance issues such as instability, phase margin limitations, and frequency response limitations. This enables the development of Op-Amps that are well-suited for portable applications, where low power consumption, small size, and high performance are critical requirements.

2. Literature Review

In 2008 KavitaKhare presented a novel input and output biasing circuit to extend the input common-mode (CM) voltage range and the output swing. The mixed-signal circuits need to operate at low voltage levels [10]. In this work a newly designed input signal compression circuit was added to the input of a folded-cascode op-amp. The compression circuit equipped rail-to-rail input, while the folded cascode op-amp has rail-to-rail output. DC Simulation of folded cascode op-amp following the input signal compression circuit using cadence spectra showed that the rail-to-rail input the signal range is compressed to the common-mode range.
In 2011 Er.Rajni designed and analyzed Folded-cascode the amplifier in 1.25μm CMOS technology [11]. At first, the work described two-stage cascode op-amp design in 1.25μm technology and it was found that the gain was not sufficient. As a remedy, the authors designed a high gain folded-cascode the simulation of the circuits was done using TSPICE simulation tool and the LEVEL–2, 1.25μm parameters. A complete analysis of the circuit has done and the simulated circuits compared together. A comparison between the cascode and folded-cascode op- amps is described. We have also described the comparison of their simulated and calculated results individually.
In 2014 Jack Ou et al. proposed a low-noise folded-cascode amplifier to explain the tradeoffs using the gm/ID design flow [12]. A 130-nm CMOS process with a 1.2-V power supply was used for this work. The specifications are a slew rate of 7.5 V/μs, a load capacitance of 100 pF, a unity bandwidth of 10 MHz, an input/output common-mode voltage of 0.6 V, current consumption of 75μA. The circuit required common-mode feedback (CMFB) with a bias current of 37.5μA. The maximum device noise corner frequency was 20 kHz [12].
In 2015 Yun Yin et al. proposed a stacked 2.4-GHz CMOS power amplifier (PA) with a mode switching scheme. With the help of dynamically harmonizing the bias and optimal load with a power-detecting controller, the proposed mode switching scheme effectively improved the power-added efficiency (PAE) of the amplifier [13]. This work used the transistor stacking and envelope tracked self-biasing techniques, to improve power amplifier efficiency effectively.
In 2017 Ramakrishna Kundu presented a two-stage fully differential, RC Miller compensated CMOS operational amplifier [14]. It could be used efficiently in a closed-loop feedback system due to high gain, and it is useful in high-speed applications due to its improved bandwidth. The circuit is implemented in 0.18 μm technology using the tool Cadence virtuoso. The designed circuit exhibited 95 dB gain, 135 MHz UGB, phase margin of 53o, with 1 pF differential capacitive load. The circuit consumed 2.29 mW from 3.3V supply.
In 2018 Andrea et al. studied the electromagnetic effects at the input stage of low power, CMOS chopped operational amplifiers [15]. In this, the authors contracted the model to describe that chopped to study nonlinear distortion effects. Moreover, the proposed models are validated by using EMI susceptibility measurements and it showed simultaneous presence of the three types of offsets in the same chopped operational amplifier.
In 2019 Ting Ma & Feng Hu presented a wideband flat gain LNA designed in 130nm CMOS technology [16]. Here the input matching is provided by an active inductor. The bandwidth obtained in this work was from 0.7 to 4.6 GHz the gain variation across the operating frequency is 1.3dB. The circuit consumed 6.16mW power with 1.4 V supply voltage.

3. Design methodology of a Low Voltage Op-Amp

The initial step in designing an operational amplifier (Op-Amp) involves selecting or creating the basic structure, which typically remains unchanged throughout the design process. However, modifications may be made if necessary. Once the structure is chosen, the next step is to select the DC currents and size the transistors, as well as design the compensation circuit. Proper scaling of the W/L ratios of the transistors is crucial to meet all AC and DC requirements imposed on the Op-Amp. Circuit simulations, combined with hand calculations, are extensively used in the design of low-voltage Op-Amp circuits.

Several factors influence the need for lower supply voltages in CMOS IC design. As the channel length decreases in CMOS technology, the maximum allowable voltage also decreases. Additionally, power dissipation is directly proportional to the number of components in the circuit, further emphasizing the need for low-voltage, low-power circuits. The demand for portable electronics, which operate on batteries, also favors lower voltage and power consumption. These factors suggest that future implementations of mixed analog/digital circuits using standard CMOS will likely require power supplies of 1.5V or less.

Figure 2 illustrates a low-voltage two-stage Op-Amp with VDD ≥ VT (threshold voltage). Many Op-Amp designs face challenges with lower power supplies, typically around 2VT. The limit of the Op-Amp at low-power-supply voltage is related to the desired input common-mode range. Thus, designing Op-Amps for operation down to VDD = 2VT requires careful consideration.

Figure 3 shows an Op-Amp designed for a voltage range down to 2VT. The input stage consists of a simple n-channel differential amplifier with current-source loads (M1, M2, M3, M4). The currents from the differential output are folded through transistors M6 and M7 and converted to single-ended signals using n-channel current mirrors (M8, M9).

To improve the second-stage gain, a miller-compensated class-A output stage is used. This Op-Amp maintains performance similar to a standard two-stage Op-Amp but can operate at lower power-supply voltages. It offers an advantage over the classical two-stage Op-Amp by having balanced loads for the input differential stage.

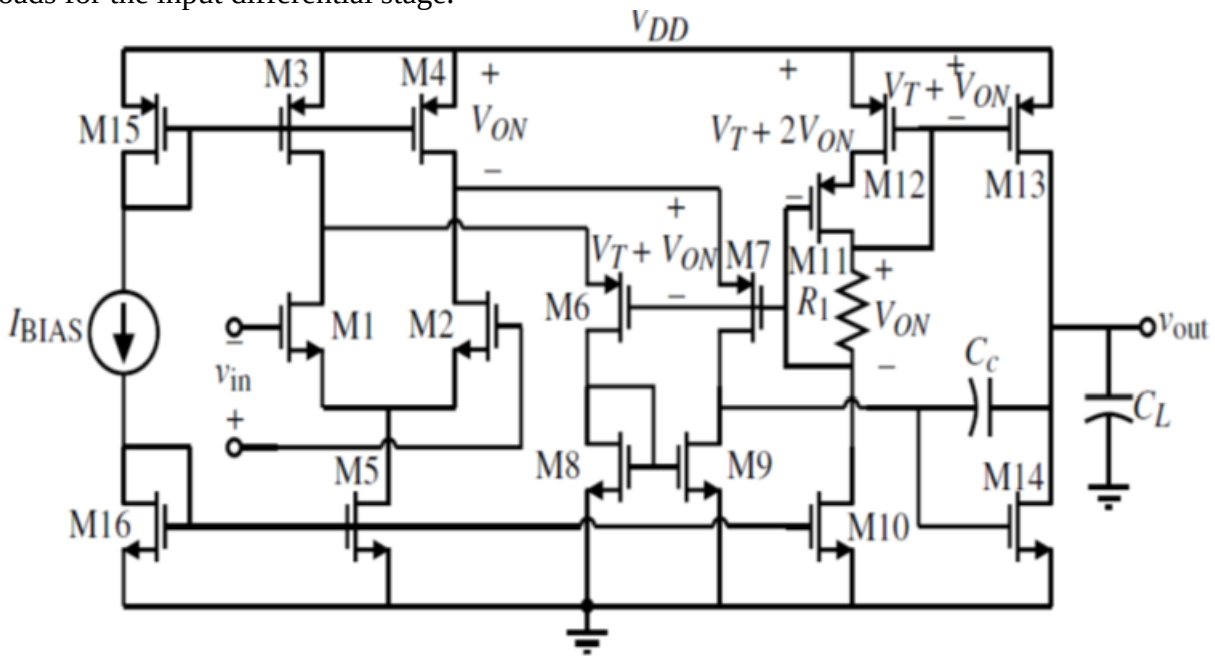


Figure 3 A Low voltage, two stage op amp with VDD ≥ VT [5]

In designing operational amplifiers (Op-Amps) for low-power-supply voltages down to VDD = 2VT, several considerations and design techniques are employed to ensure optimal performance. The Op-Amp architecture shown in Figure 3 is a two-stage design that incorporates specific features to achieve this goal.

1. Input Stage: The input stage is a simple n-channel differential amplifier with current-source loads (M1, M2, M3, M4). This stage amplifies the differential input signal and provides it to the subsequent stages of the Op-Amp. The use of current-source loads helps improve the linearity and gain of the amplifier.

2. **Current Folding:**The currents from the differential output are folded through transistors M6 and M7. This folding technique is commonly used in low-power Op-Amps to reduce power consumption and improve efficiency.

3. Single-Ended Signal Conversion: The folded currents are then transformed to single-ended signals using n-channel current mirrors (M8, M9). This conversion is essential for further processing and amplification of the signal in subsequent stages.

4. Miller Compensation: To improve the gain and stability of the second stage, a miller-compensated class-A output stage is employed. Miller compensation is a common technique used in Op-Amps to enhance stability and bandwidth while maintaining a high gain.

5. **Balanced Input Differential Stage:**One of the advantages of this Op-Amp design is that the loads of the input differential stage are balanced. This helps improve thecommon-mode rejection ratio (CMRR) and reduces distortion in the amplifier's output.

The design of Op-Amps for low-power-supply voltages requires careful consideration of various factors, including transistor sizing, compensation techniques, and overall circuit architecture. By employing these design techniques, it is possible to achieve high performance and efficiency in Op-Amps operating at low supply voltages.

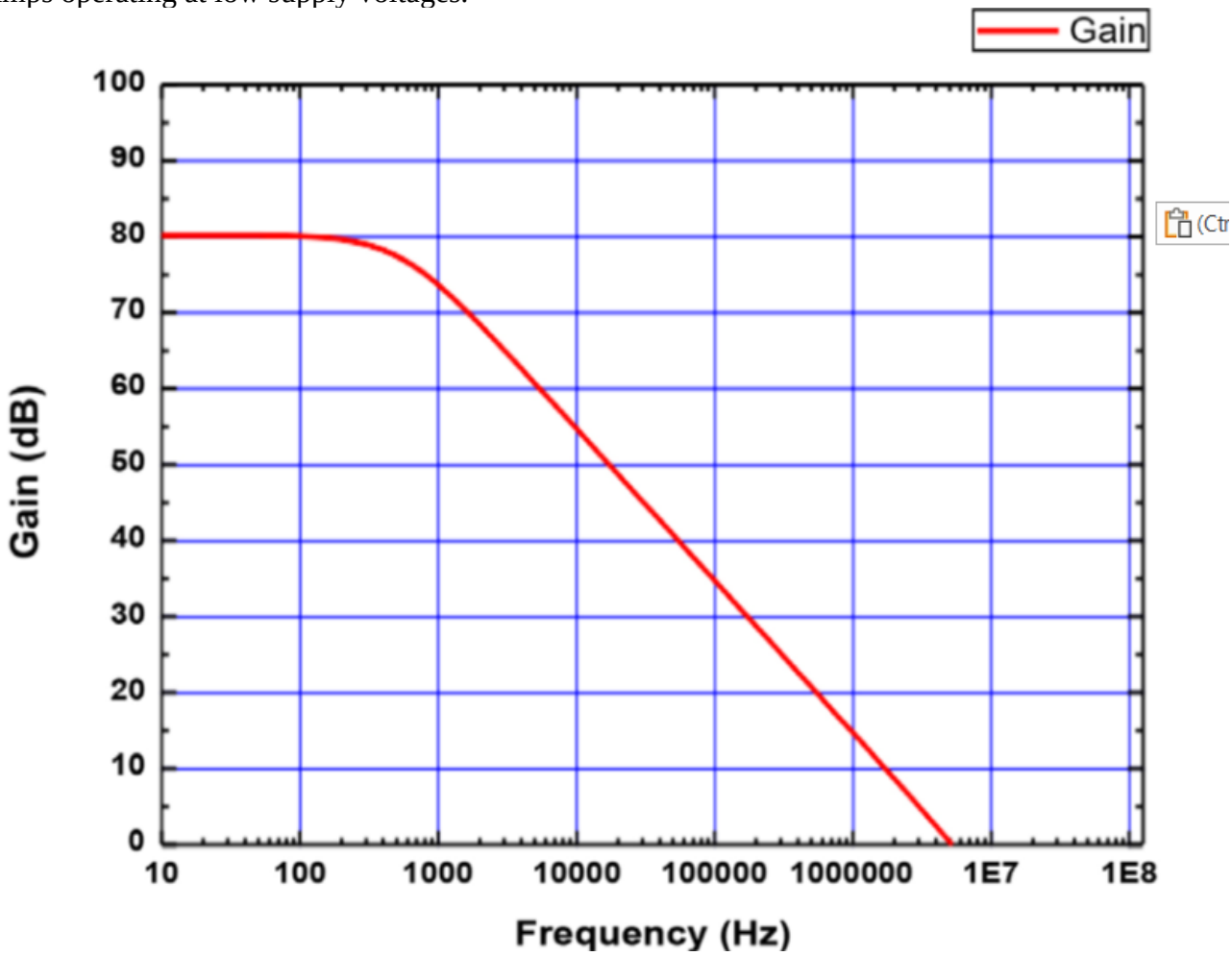


Figure 3Frequency response of two stage Op-Amp

In designing an operational amplifier (Op-Amp), especially for low-voltage applications, the choice of compensation capacitance (Cc) is crucial for ensuring stability and proper frequency response. It is generally recommended that Cc be larger than the load capacitor (CL) to maintain stability. Additionally, the transconductance of the output device should be sufficient to ensure that the second pole does not significantly degrade the frequency response.

However, increasing Cc comes at a cost of higher power consumption. This is because the compensation capacitance directly affects the power consumption of the Op-Amp. Therefore, there is a trade-off between stability and power consumption, and designers must carefully optimize these parameters based on the specific requirements of the application.

The Op-Amp design was simulated using the LTspice simulation tool, which is widely used for simulating electronic circuits. The simulation results provide valuable insights into the performance of the Op-Amp in different CMOS process technologies.
Figure 3 illustrates the simulated frequency response of the two-stage Op-Amp in a 0.25μm CMOS linear technology in LTspice. The graph shows the gain and phase characteristics of the Op-Amp over a range of frequencies. Additionally, the frequency response of the proposed low-voltage Op-Amp was simulated in a 0.15-μm CMOS process, as shown in the same figure.
The simulation results indicate that the low-frequency gain of the Op-Amp is approximately 49.18 dB, and it has a phase margin of 65.14˚ with a load capacitor of 10 pF. These results demonstrate that the designed Op-Amp meets the stability and performance requirements for low-voltage applications, making it suitable for use in portable electronics and other low-power applications.

4. Results and Discussion

In switched-capacitor circuits and linear CMOS circuits, operational amplifiers (op-amps) serve as essential building blocks for signal processing, amplification, and conditioning. The ideal op-amp, though theoretical, is conceptualized as a perfect voltage-controlled voltage source with infinite voltage gain, zero input admittance, and zero output impedance. This ideal op-amp is assumed to exhibit no frequency or temperature dependence, distortion, or noise, making it a highly desirable component in circuit design.
However, practical op-amps have limitations and imperfections. A detailed block diagram of a Metal-Oxide-Semiconductor (MOS) op-amp is provided in Figure 3, with a more comprehensive depiction presented in Figure 4. This op-amp configuration typically consists of multiple stages:
1. **Differential Stage (G1):** This stage amplifies the voltage difference between the input terminals (differential input) and is responsible for providing most of the op-amp's voltage gain.
2. **Single-Ended Stage (G2):** Following the differential stage, the single-ended stage further amplifies the signal and converts it to a single-ended output. This stage ensures compatibility with single-ended loads and applications.
3. **Output Stage (G3):** The output stage acts as a buffer, providing a low-output-impedance unity-gain output. It is designed to drive large capacitive and resistive loads effectively.

In switched-capacitor circuits, where capacitors play a significant role in signal processing, the op-amp's role may differ slightly. For internal stages of such circuits, where the load typically consists of small capacitors (2 pF or less), the output buffer (G3) may be unnecessary. In this scenario, the load can be connected directly to the output of the single-ended stage (G2), effectively transforming the op-amp into an operational transconductance amplifier (OTA). Similarly, if the differential stage (G1) provides sufficient gain and output voltage swing, the single-ended stage (G2) can be omitted, allowing the load to be driven directly by the differential stage.
These configurations illustrate the adaptability of op-amps in various circuit designs, allowing for optimization based on specific application requirements. While the ideal op-amp remains a theoretical concept, practical op-amp designs strive to minimize imperfections and achieve high performance in real-world applications.

5. Conclusions

In this work, the focus is on the design and performance of a two-stage CMOS op-amp tailored for biomedical applications, with specific attention given to achieving high gain and bandwidth in both 180nm and 90nm technologies.
1. **Op-Amp Design Overview:**The op-amp design consists of three main stages: a differential amplifier, a gain stage (common source), and an output buffer. The differential amplifier (first stage) is formed by transistors M1 and M2, while the current mirror load is provided by transistors M3 and M4. The second stage is the gain stage, comprising transistors M6 and M7. The biasing for the entire circuit is provided by transistor M5.
2. **Achieved Performance Metrics:**The design achieved an impressive open-loop gain of 21.25 dB and 26.26 dB for the 180nm and 90nm technologies, respectively. Additionally, the unity gain bandwidth was measured at 9.78 MHz and 5.05 MHz for the two technologies. These values

represent significant improvements over previous designs and demonstrate the effectiveness of the proposed approach.

3. Impact of Technology Scaling:A key observation from the comparative analysis is the impact of scaling on the op-amp performance. While the gain is higher in the 90nm technology by 5.31 dB, the unity gain bandwidth is almost two times higher in the 180nm technology compared to the 90nm technology. This highlights the trade-offs involved in technology scaling and the need for careful consideration in design.

4. **Biomedical Applications and FinFET Technology:**The study also discusses the relevance of FinFET technology in biomedical applications. FinFETs offer superior gate control and reduced leakage currents compared to traditional CMOS technology. The gate electrode in FinFETs wraps around the channel, allowing for multiple gate electrodes on each side, leading to improved performance in biomedical applications.

In conclusion, this work demonstrates the successful design of a two-stage CMOS op-amp for biomedical applications, achieving high gain and bandwidth in both 180nm and 90nm technologies. The study also highlights the importance of technology scaling and the potential benefits of FinFET technology in biomedical device design.

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